REMARKS

In the Office Action dated August 25, 2004, the Examiner rejected claims 1-6, 8, 11, 12 and 14 under 35 USC 102(e) as anticipated by Shinohara (U.S. Patent No. 6,358,778), rejected claims 1-5, and 7-14 under 35 USC 102(e) as anticipated by Wang (US Patent 6,258,626), rejected claims 9, 10 and 13 under 35 USC 103 as unpatentable over Shinohara and Wang, and rejected claims 9, 10 and 13 under 35 USC 103 as unpatentable over Satsu (US Patent 6,762,511) and Wang. In response thereto, the Applicant has amended claims 1 and 11. New claims 16 through 21 have been added. Claims 1 through 21 remain at issue..

35 USC 102 Rejections

The Shinohara reference teaches a chip package having a lead frame 1 with a plurality of terminals 2. A semiconductor device 4 is mounted onto the lead frame 1 using electrically conductive bumps 12 between electrodes on the device 4 and the terminals 2. Once the device 4 is mounted onto lead frame, it is then individually encapsulated in a sealing resin 7. The lead frame is then mechanically cut to singulate the package. See Figures 4A-4C and column 5, lines 34-67.

Wang discloses a stacked chip package including a first chip 110 mounted onto a substrate 120 with "flip chip" pads 124 and wire bond pads 122. Solder joints 112 are used to mount a first chip onto the flip chip pads 124 of the substrate. A second chip 130 is then mounted onto the first chip 110. Wire bonds are formed between the second chip 130 and the wire bond pads 122.

The present invention as claimed covers a semiconductor package having lead frame with a plurality of lead posts. Each of the plurality of lead posts are positioned on a plurality of lead fingers respectively. The lead fingers are electrically isolated from one another by encapsulant.

On the other hand, Shinohara teaches only the use of terminals. There is no teaching whatsoever regarding lead fingers. The Shinohara reference fails to teach or suggest the use of lead frame fingers.

The Wang reference also fails to teach or suggest the use of (i) a lead frame; (ii) lead posts; or (iii) lead fingers. On the contrary, the solder joints 112 of Wang are not posts. The substrate 120 of Wang is not a lead frame.

For the reasons specified above, claims 1-10 and 11-15 are allowable.

The applicant has added new claims 16-18 which are directed to a lead frame having a substantially continuous and planar second surface to prevent encapsulant material from forming on the bottom surface of the package. Bottom surface of Shinohara is neither continuous or planar. On the contrary, the second surface is perforated or "punched" with a die to form the terminals 12. See Column 4, lines 12-24. The package of Wang fails to teach at all the use of a lead frame, let alone a substantially planar and continuous lead frame.

The applicant has also added new claims 19-21 which are directed to a encapsulating a plurality of semiconductor die mounted onto the posts of a lead frame. The lead frame has a second substantially planar second surface to prevent encapsulant material from forming on the bottom surface of the package. Figure 4A of Shinohara clearly shows that die are individually encapsulated on the lead frame 10. Furthermore, the bottom surface of Shinohara is neither continuous or planar. On the contrary, the second surface is perforated or "punched" with a die to form the terminals 12. See Column 4, lines 12-24. The package of Wang fails to teach at all the use of a lead frame or the encapsulation of the two stacked chip package.

It is respectfully submitted that all pending claims are allowable and that this case is now in condition for allowance. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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